

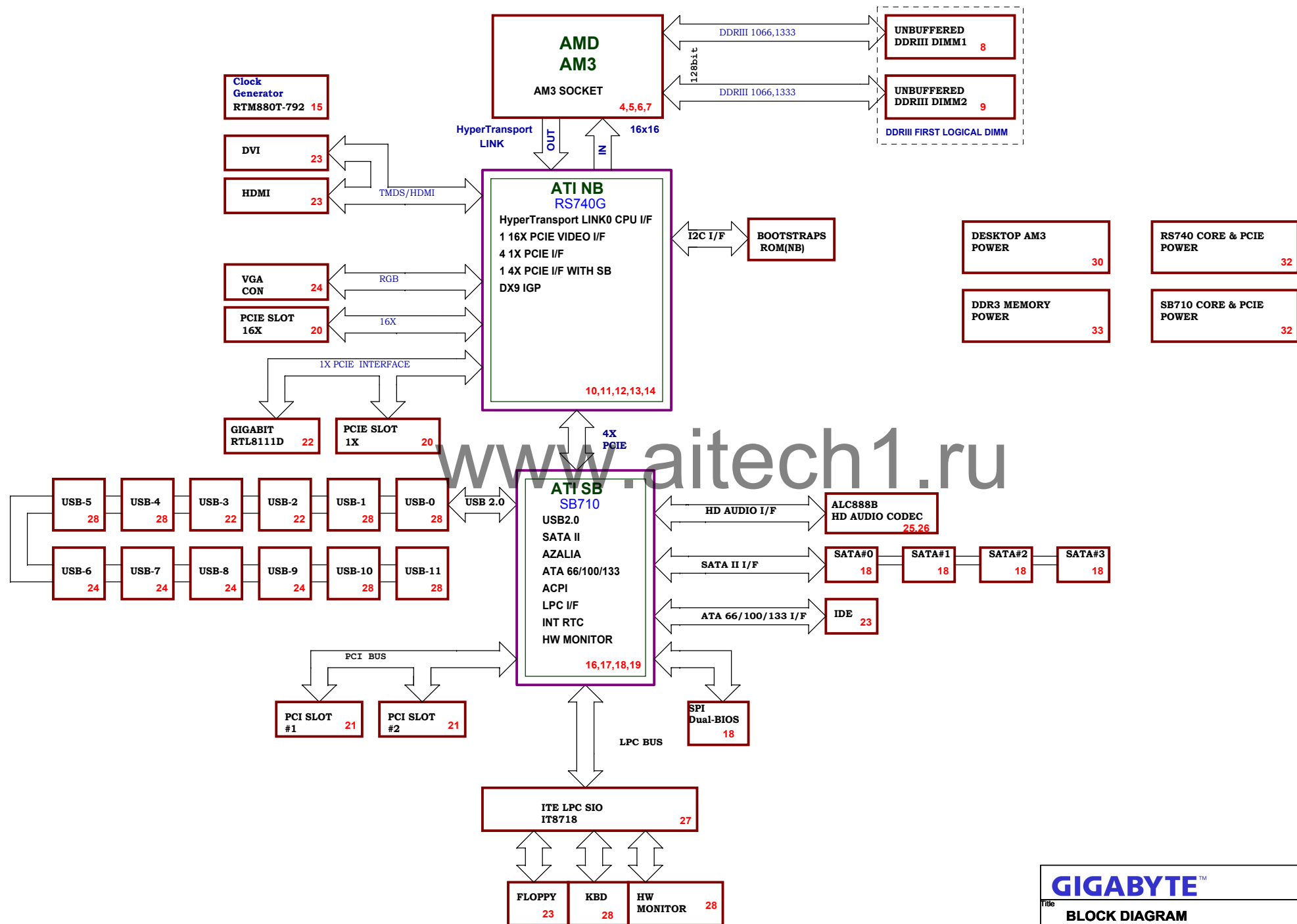
**Revision : 1.3**

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11	RS740 PCIE I/F
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17	ATI SB710 ACPI/USB/GPIO/AUDIO
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22	REALTK RTL8111D/8103E
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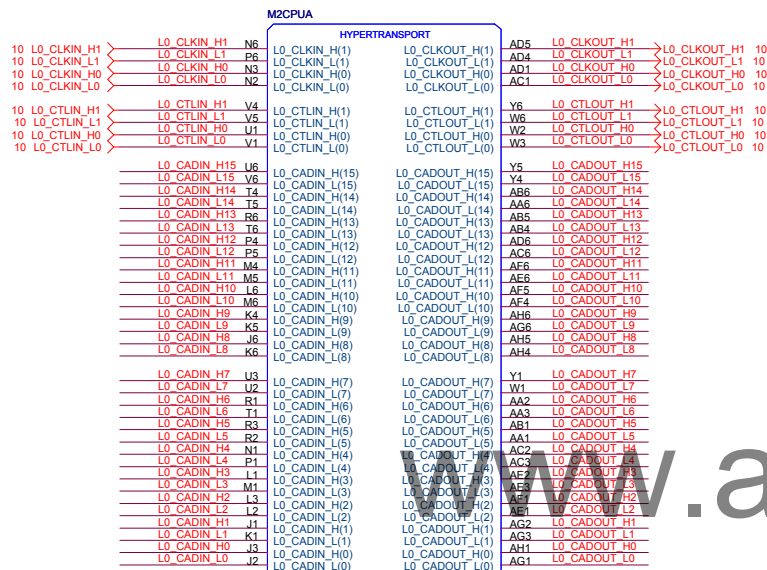
[illegible]

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## RS740 CUSTOMER DESKTOP REFERENCE DESIGN



L0\_CADIN\_L[0..15] < L0\_CADIN\_L[0..15] 10  
L0\_CADIN\_H[0..15] < L0\_CADIN\_H[0..15] 10  
L0\_CADOUT\_L[0..15] < L0\_CADOUT\_L[0..15] 10  
L0\_CADOUT\_H[0..15] < L0\_CADOUT\_H[0..15] 10



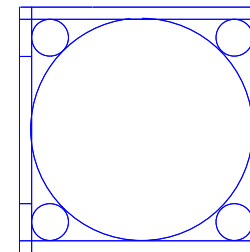
CPU-SK941AM3S/GF[10SC1-A01941-01R]

CPU\_VDD\_RUN = VCORE  
CPU\_VDDA\_RUN = VDDA25  
VLDT\_RUN = VCC12\_HT  
CPU\_VDDIO\_SUS = DDR15V  
CPU\_VDDR = CPU\_VDDR12

VLDT\_A = VCC12\_HT  
VLDT\_B = HT12B

M2CPU

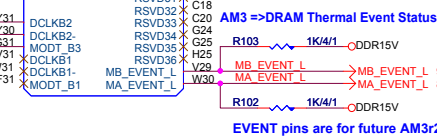
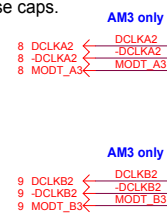
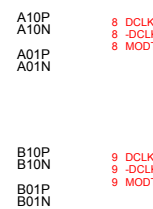
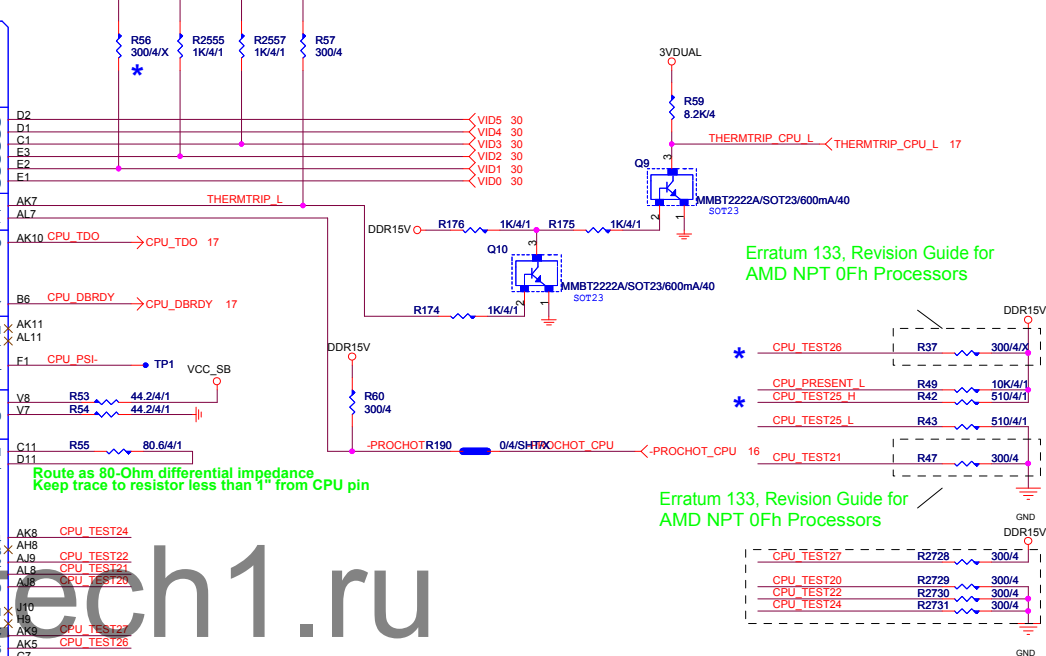
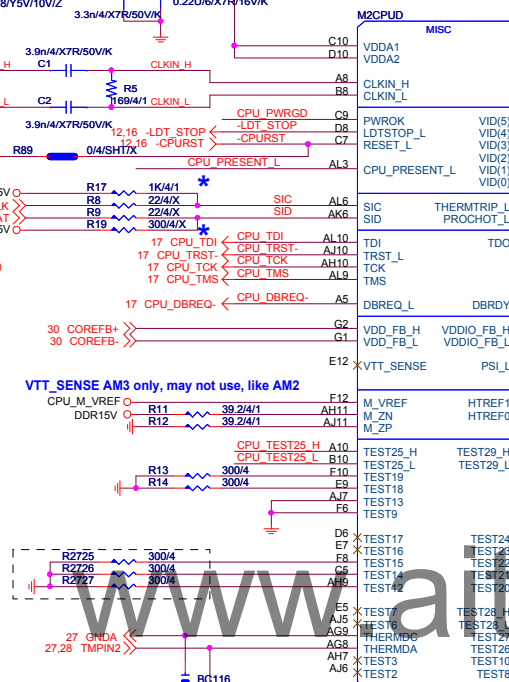
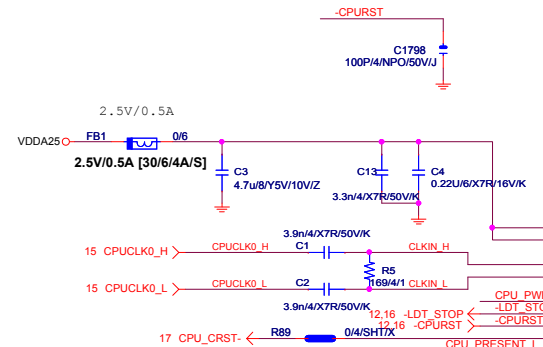
AM2RM/PP/BU/PB[12KRC-04K812-11R]



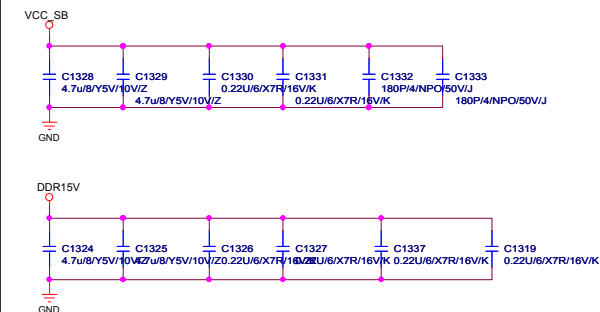
**GIGABYTE™**

Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-MA74GMT-S2	1.3	
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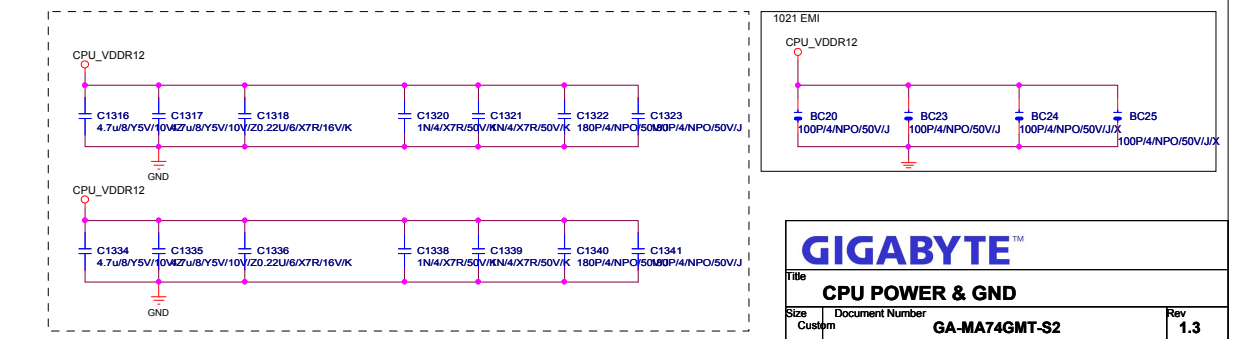


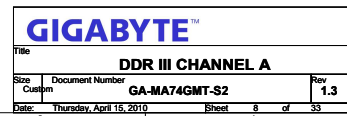


**Layout: Route as 60 ohms  
with 5/10 W/S from CPU pins.**



H22 Missing pins on package and socket used for mechanical keying. =>AM3



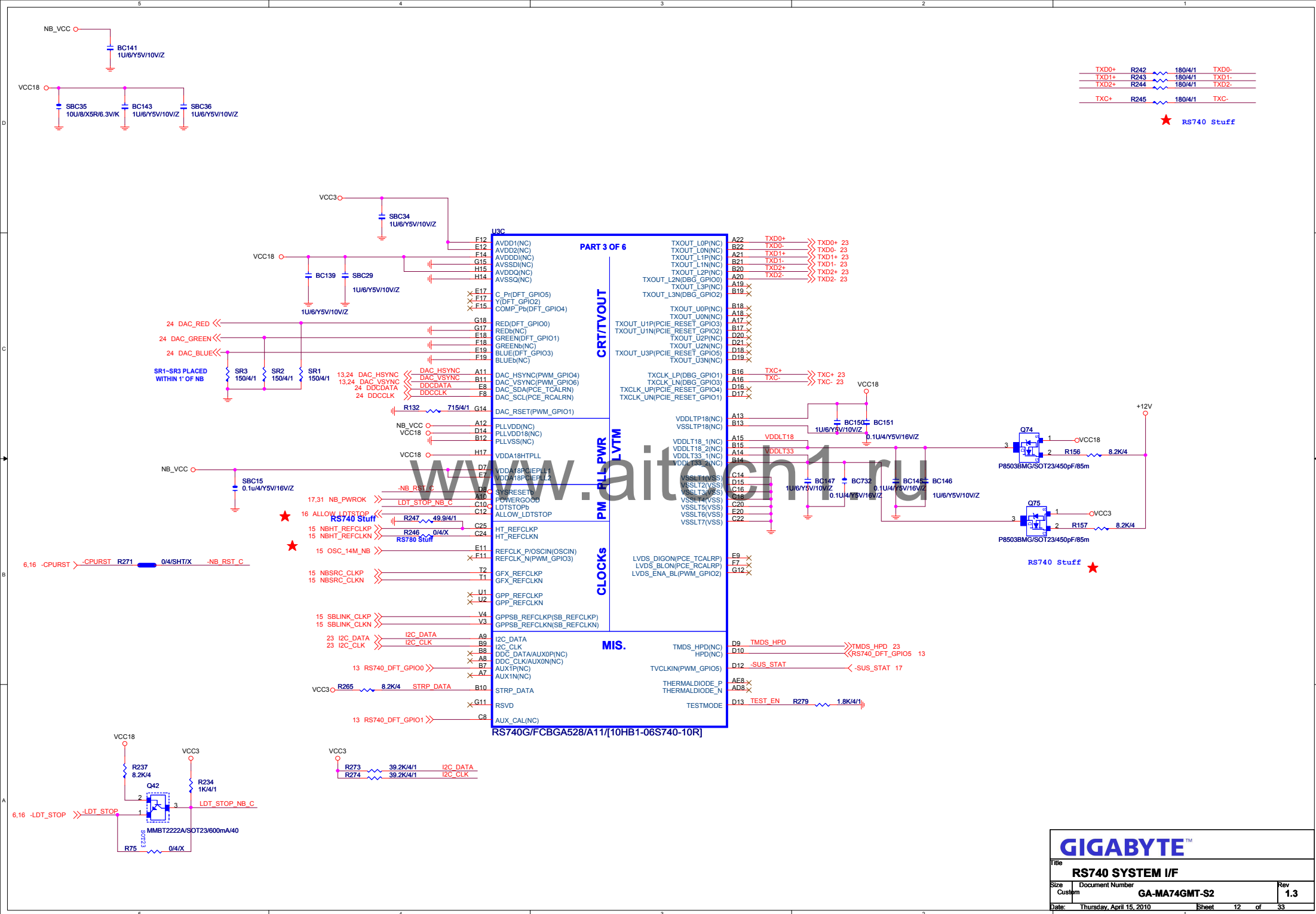


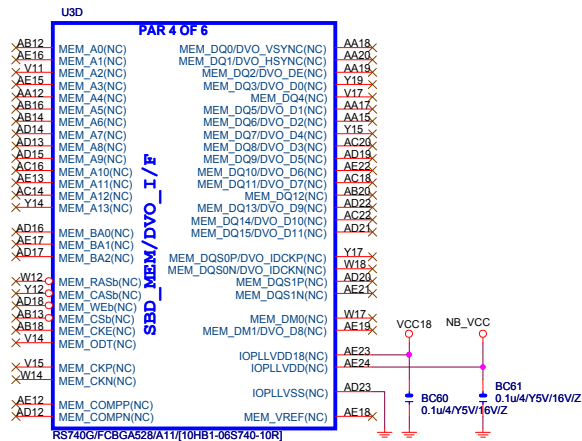












## RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX\_CAL, place close to pin C8

12 RS740\_DFT\_GPIO1 >> R272 150/4/1X RS740 non-Stuff

Note: for RX780, R217 (RX780\_DFT\_GPIO1) to 3K accordingly

12,24 DAC\_VSYNC << R276 3K/4/1X VCC3  
12 RS740\_DFT\_GPIO5 >> R280 3K/4/1 RS740 Stuff VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly  
R912 (RX780\_DFT\_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly  
R913 (RX780\_DFT\_GPIO4)  
R218 (RX780\_DFT\_GPIO3)  
R911 (RX780\_DFT\_GPIO2)

12 RS740\_DFT\_GPIO0 >> R288 3K/4/1X VCC3  
12,24 DAC\_HSYNC << R285 3K/4/1X RS780 Stuff VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly  
R219 (RX780\_DFT\_GPIO0)

## RS740/RX780/RS780: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
RS740: pin DFT\_GPIO1  
RX780: pin DFT\_GPIO1  
RS780: pin SUS\_STAT#

## RS740/RX780/RS780: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO  
1 : Disable (RS740/RS780); Enable (RX780)  
0 : Enable (RS740/RS780); Disable (RX780)  
RS740: pin DFT\_GPIO5  
RX780: pin DFT\_GPIO5  
RS780: pin VSYNC

## RS740: STRAP\_PCIE\_SB/GPP\_CFG[2:0] (Pins: RS740\_DFT\_GPIO[4:2])

These pin straps are used to configure PCI-E GPP mode.  
111: register defined (register default to Config E) default  
110: 4-0-0-0-0 Config A  
101: 4-4-0-0-0 Config B  
100: 4-2-2-0-0 Config C  
011: 4-2-1-1-0 Config D  
010: 4-1-1-1-1 Config E  
others: register defined (default to Config E)

## RX780: STRAP\_PCIE\_GPP\_CFG[2:0] (Pins: RX780\_DFT\_GPIO[4:2])

111: 1-1-1-1-1 Mode L default  
110: 1-1-1-1-1 Mode L  
101: 2-0-2-0-2-0 Mode C2  
100: 2-0-2-0-1-1 Mode K  
011: 2-0-1-1-1-1 Mode E  
010: 1-1-1-1-1-1 Mode L  
001: 4-0-0-0-1-1 Mode C  
000: 4-0-0-0-2-0 Mode B

## RS780: STRAP\_PCIE\_GPP\_CFG[2:0] (configure thru register setting)

1-1-1-1-1-1 Mode L default  
1-1-1-1-1-1 Mode L  
2-0-2-0-2-0 Mode C2  
2-0-2-0-1-1 Mode K  
2-0-1-1-1-1 Mode E  
1-1-1-1-1-1 Mode L  
4-0-0-0-1-1 Mode C  
4-0-0-0-2-0 Mode B

## RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

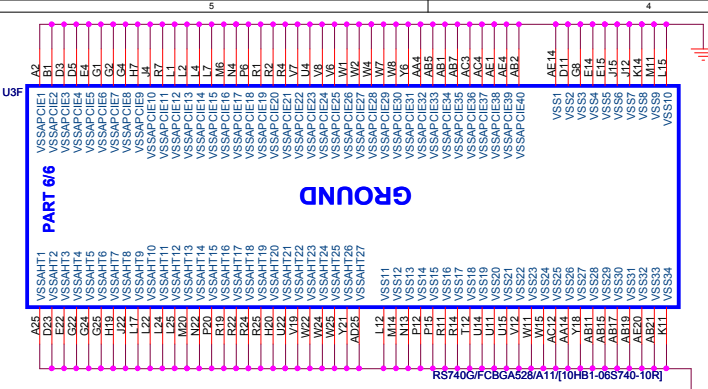
Enables Side port memory  
1. Disable (RS740/RS780)  
0 : Enable (RS740/RS780)  
RS740: pin DFT\_GPIO0  
RS780: pin HSYNC  
RX780: Not Applicable

## RX780/RS780: STRAP\_DEBUG\_BUS\_PCIE\_ENABLE

Enables Test debug bus using PCIE bus  
1. Disable (can be enabled thru nbcfg register)  
0 : Enable  
RX780: pin DFT\_GPIO0  
RS780: configurable thru register setting only  
RS740: Not supported

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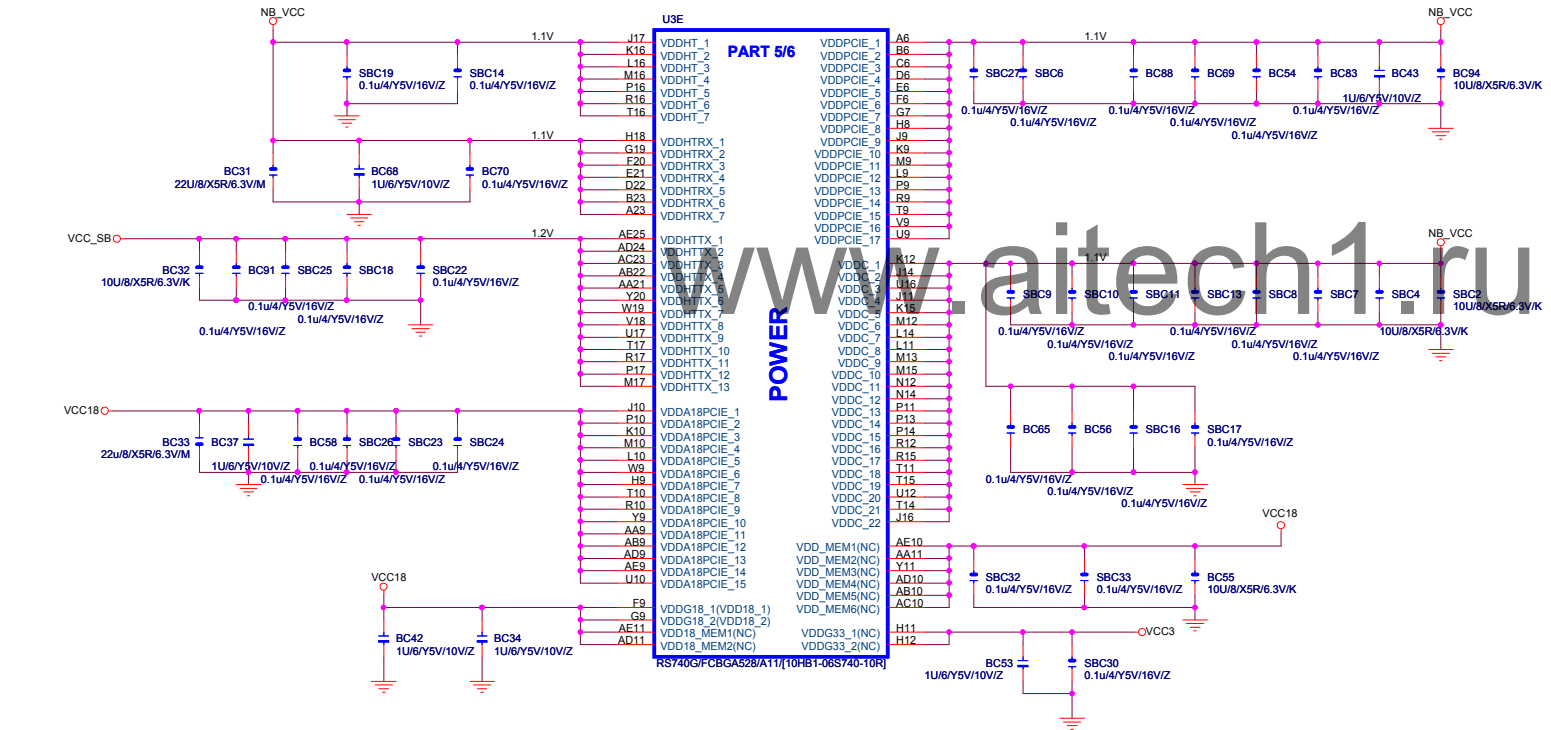
Title		
RS740 STRAP		
Size	Document Number	Rev
Custom	GA-MA74GMT-S2	1.3
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Please use 1mm pad size,  
place all ELT test pads  
on bottom side only

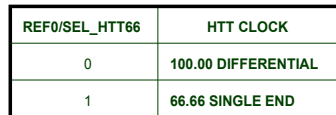
RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP18	+1.8V	NC	+1.8V





- |                         |                 |
|-------------------------|-----------------|
|                         | OSC_14M_NB      |
| RS740                   | 3.3V 33R serial |
| RX780                   | 1.8V 82.5R/130R |
| RS780<br>(Single-ended) | 1.1V 158R/90.9R |



REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

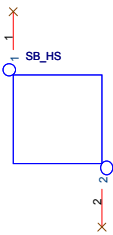
NB_CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	68M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P				
	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* the GFX\_REFCLK input is required for all cases

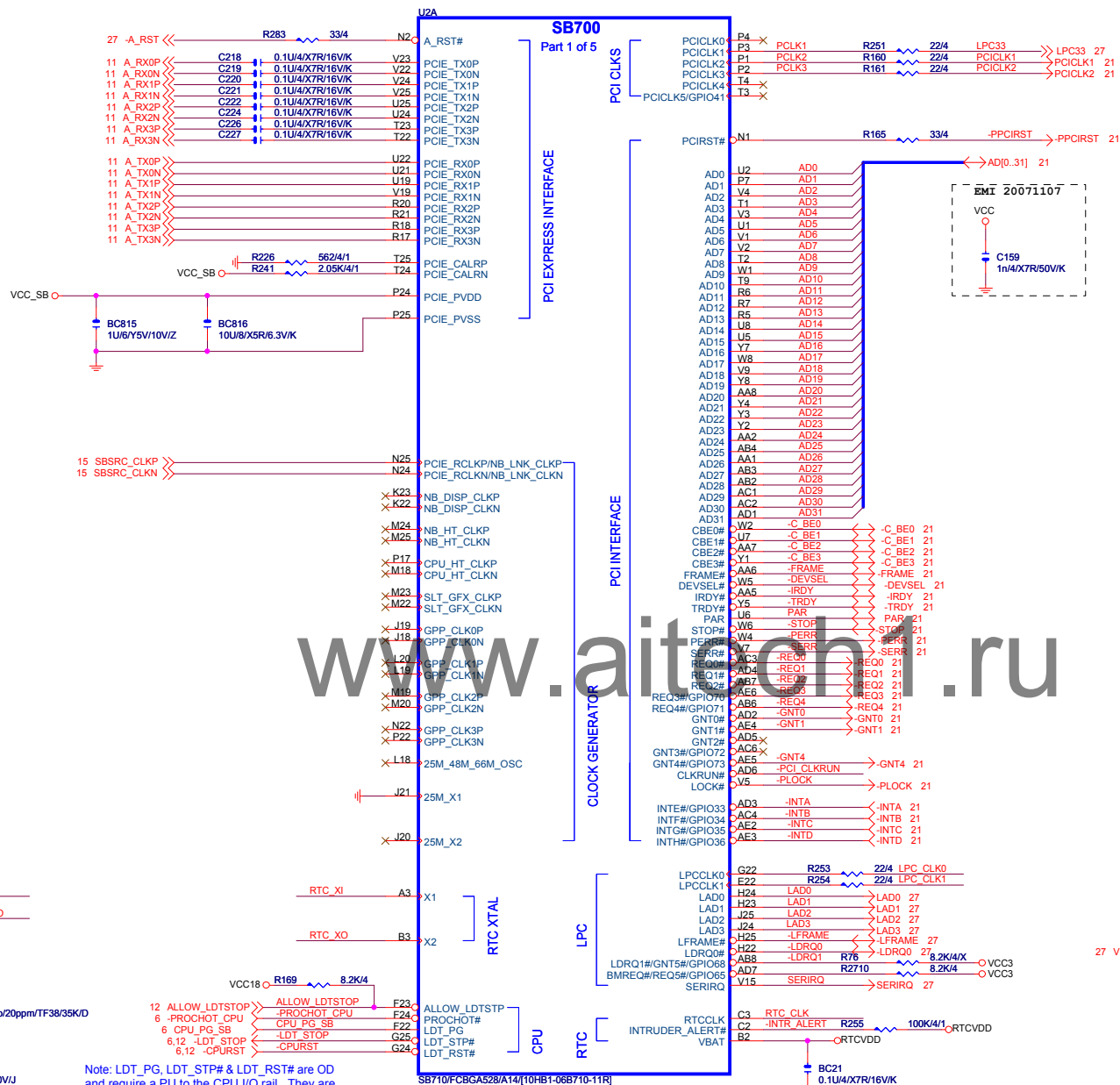


PLACE THESE PCIE AC COUPLING  
CAPS CLOSE TO U600

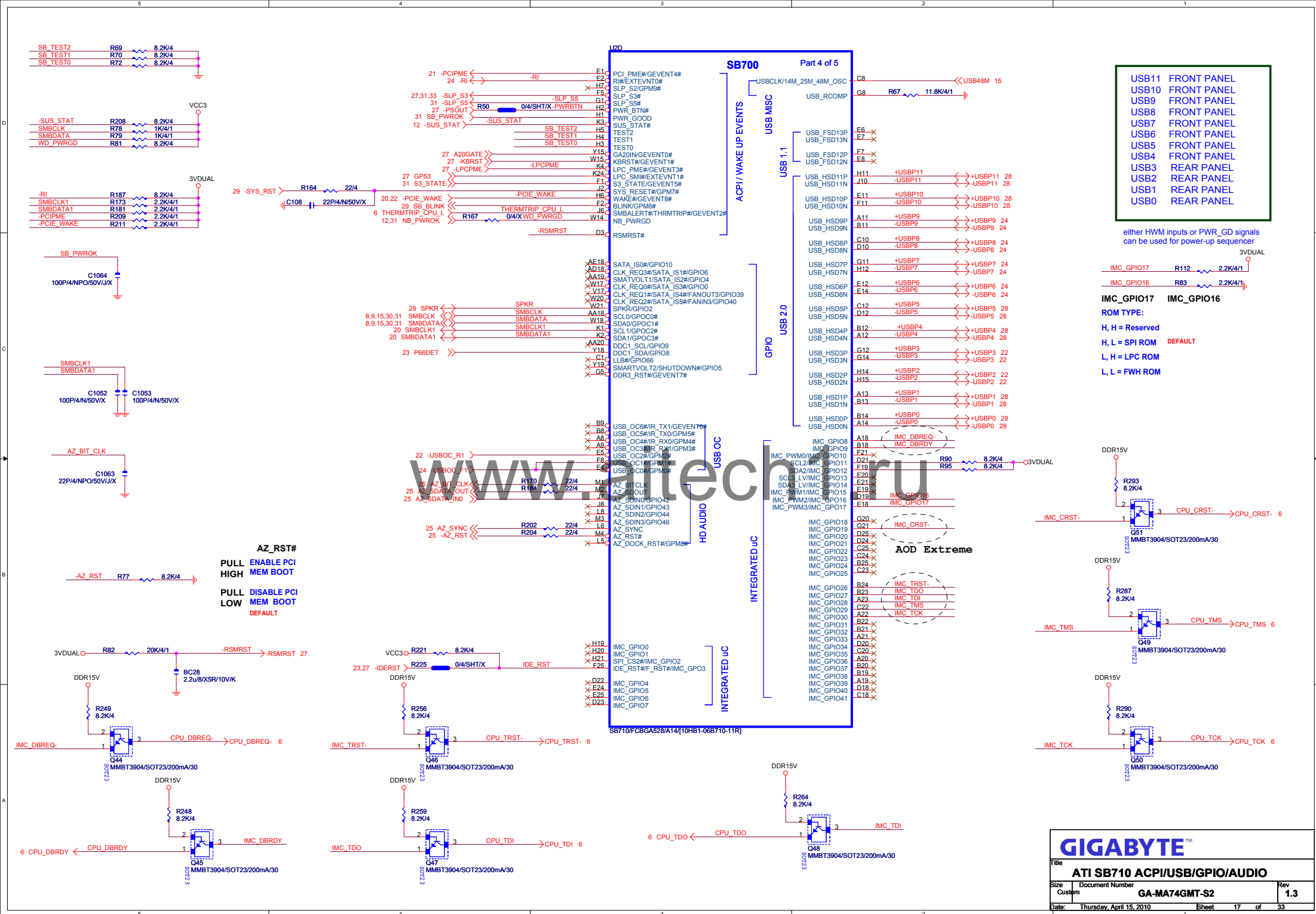
## S.B HEATSINK

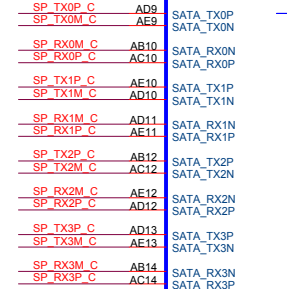
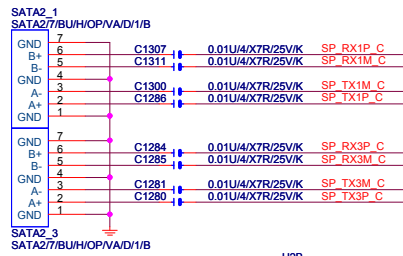
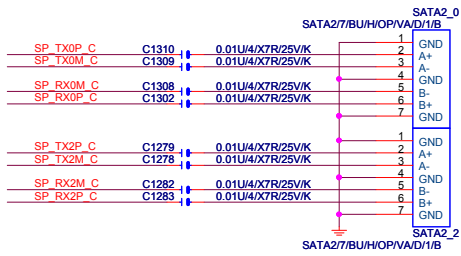


SB\_HS[12SP2-030005-42R\_12SP2-030005-43R]









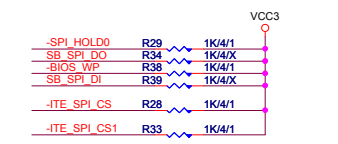
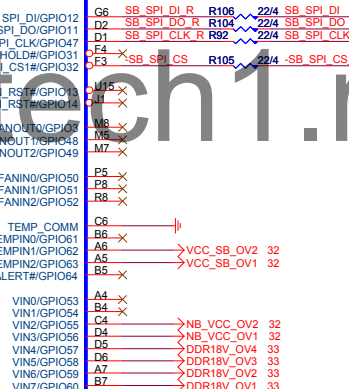
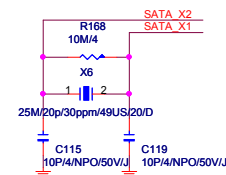
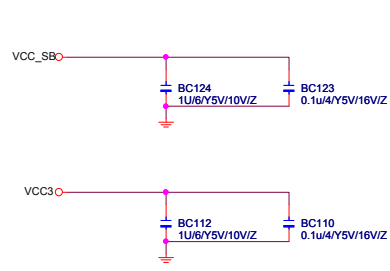
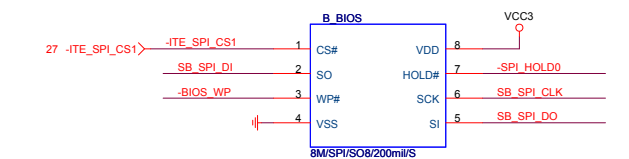
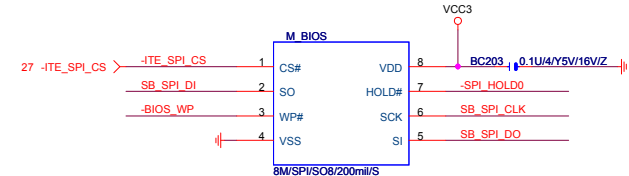
SERIAL ATA

ATA 66/100/133

SPIROM

HW MONITOR

SATA PWR

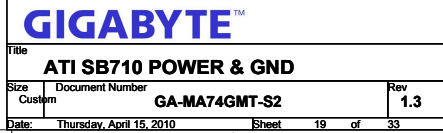


**GIGABYTE**™

Title **ATI SB710 SATA/IDE/HWM/SPI**

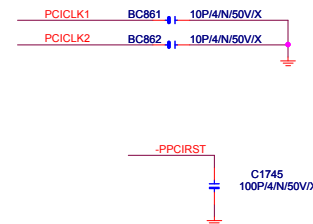
Size Custom Document Number **GA-M74GMT-S2** Rev **1.3**

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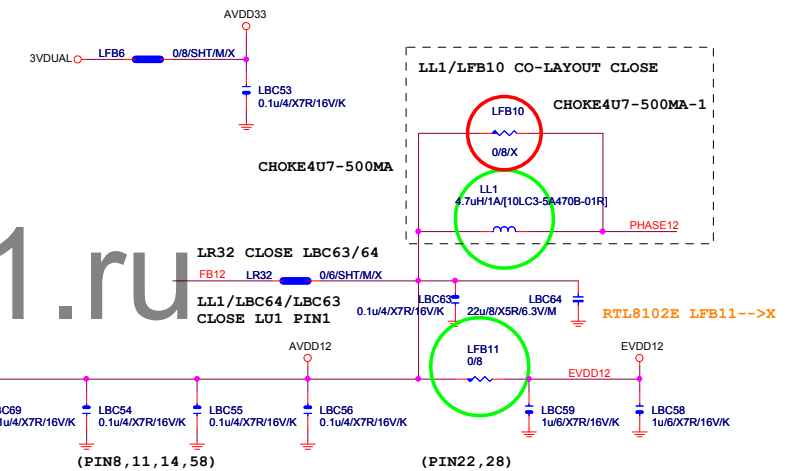
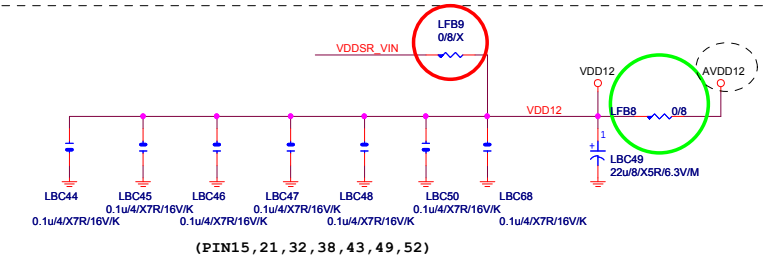
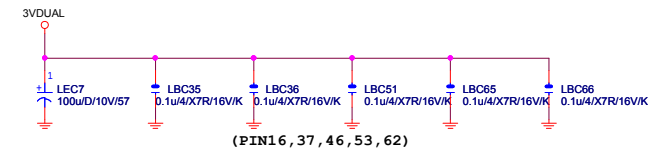
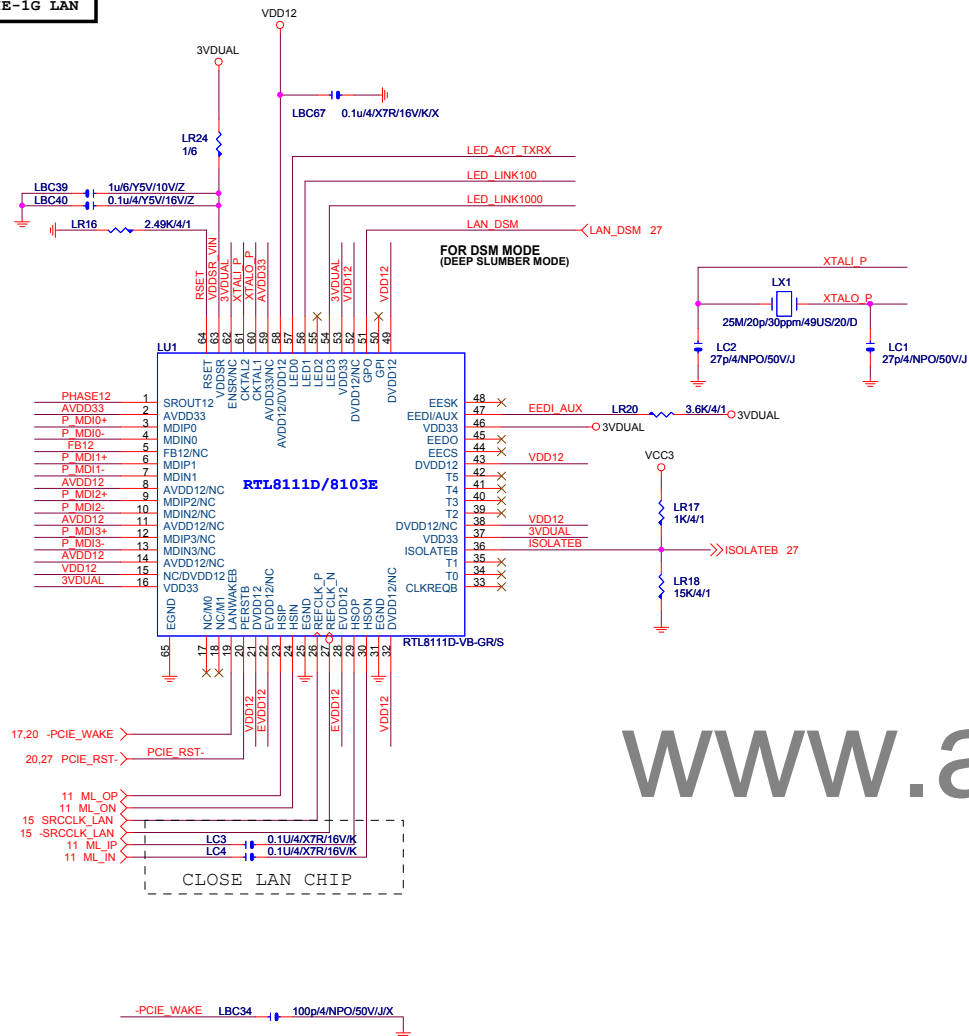


**PCI SLOT2**



Title			
<b>PCI SLOT 1,2</b>			
Size	Document Number	Rev	
Custom	<b>GA-M74GMT-S2</b>	<b>1.3</b>	
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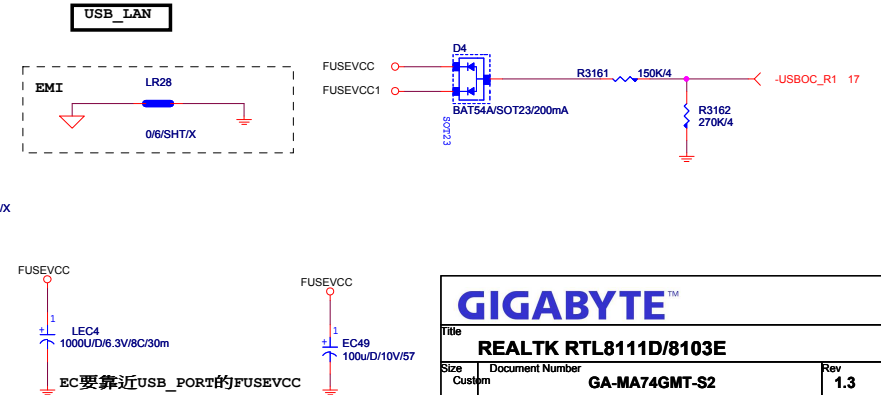
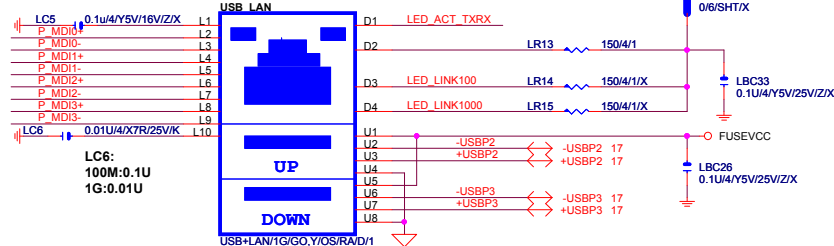
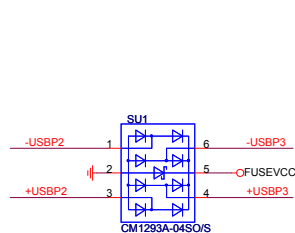
## PCIE-1G LAN



USB\_LAN CONNECTOR

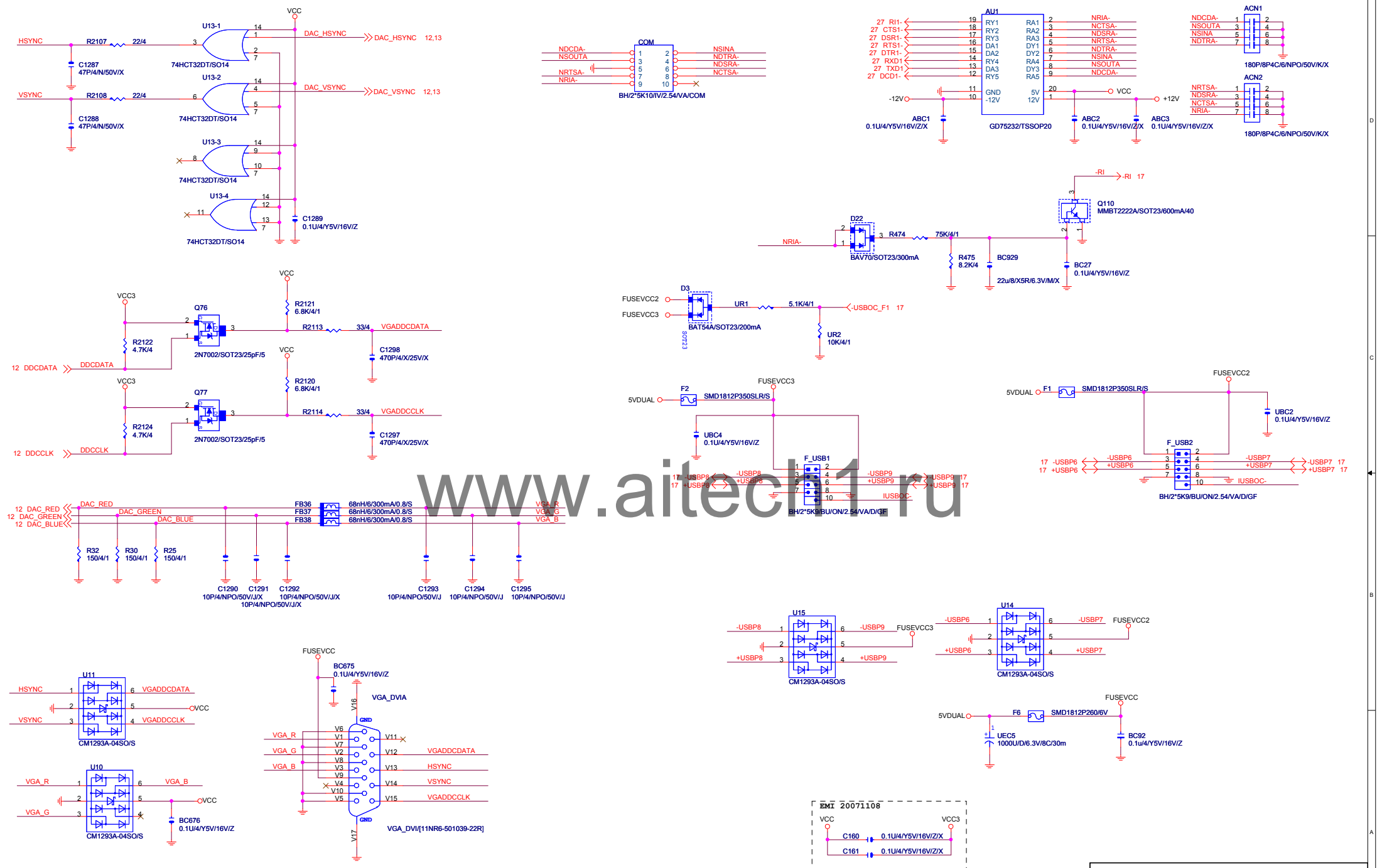
```
RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
```

```
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
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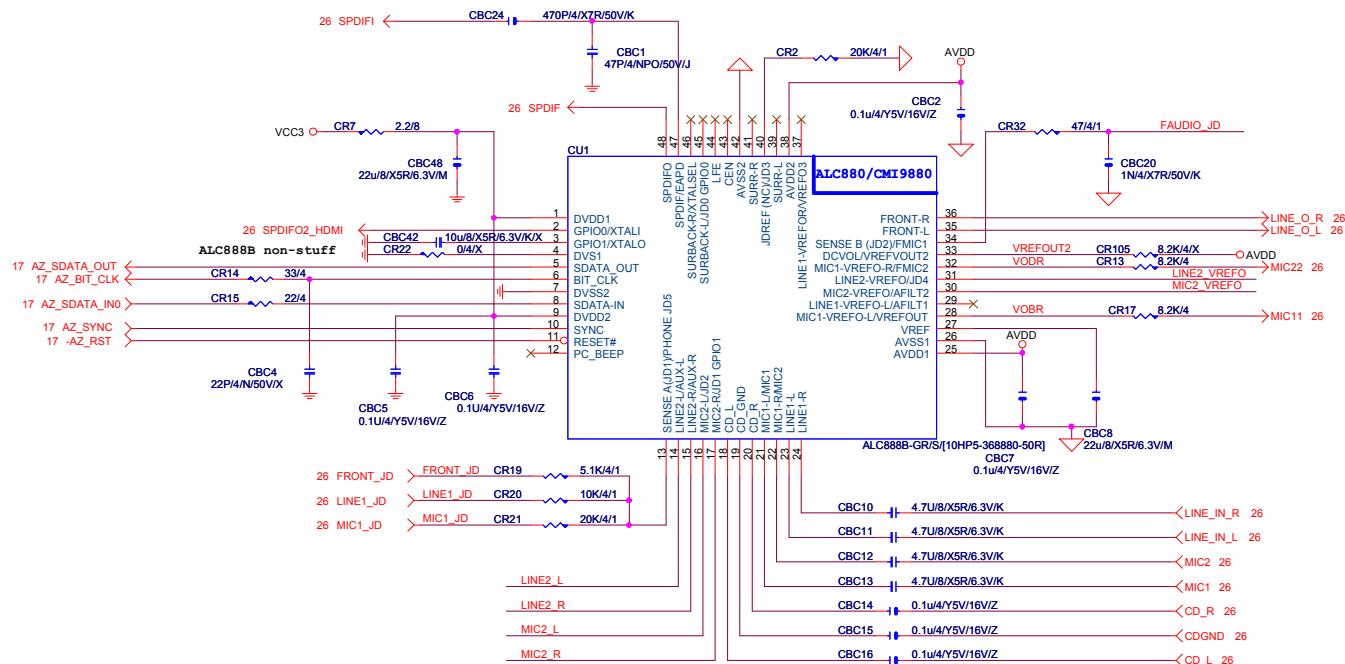






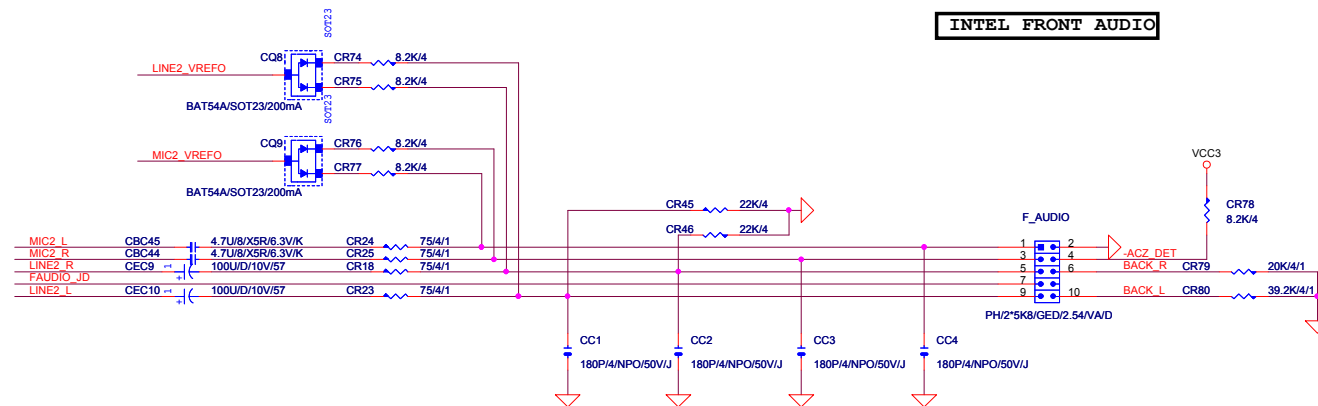


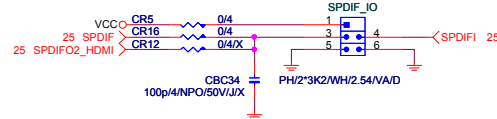
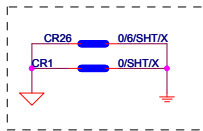




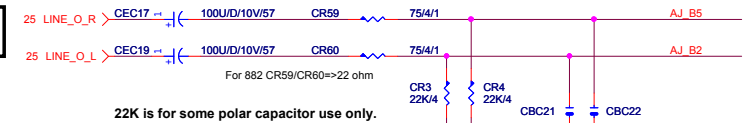
AZALIA CODEC		ALC892	ALC888B
CR22		X	X
CBC42		10uF/x5R	X
CR12		O	X
CR16		X	O

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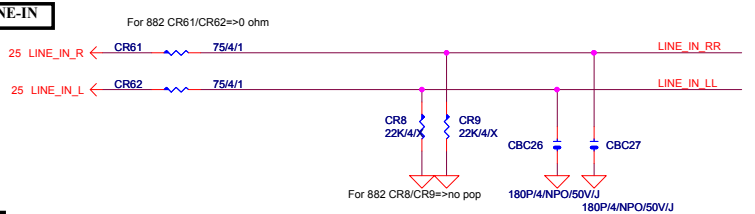




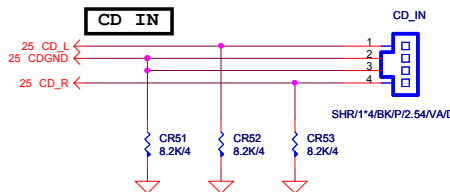
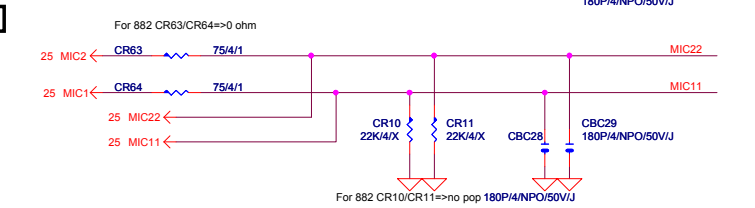
# LINE OUT FRONT OUT



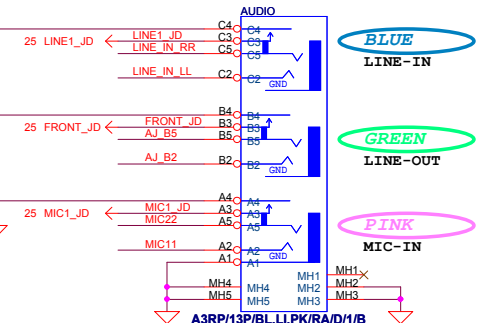
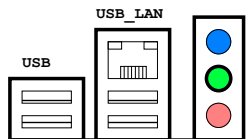
# LINE-IN



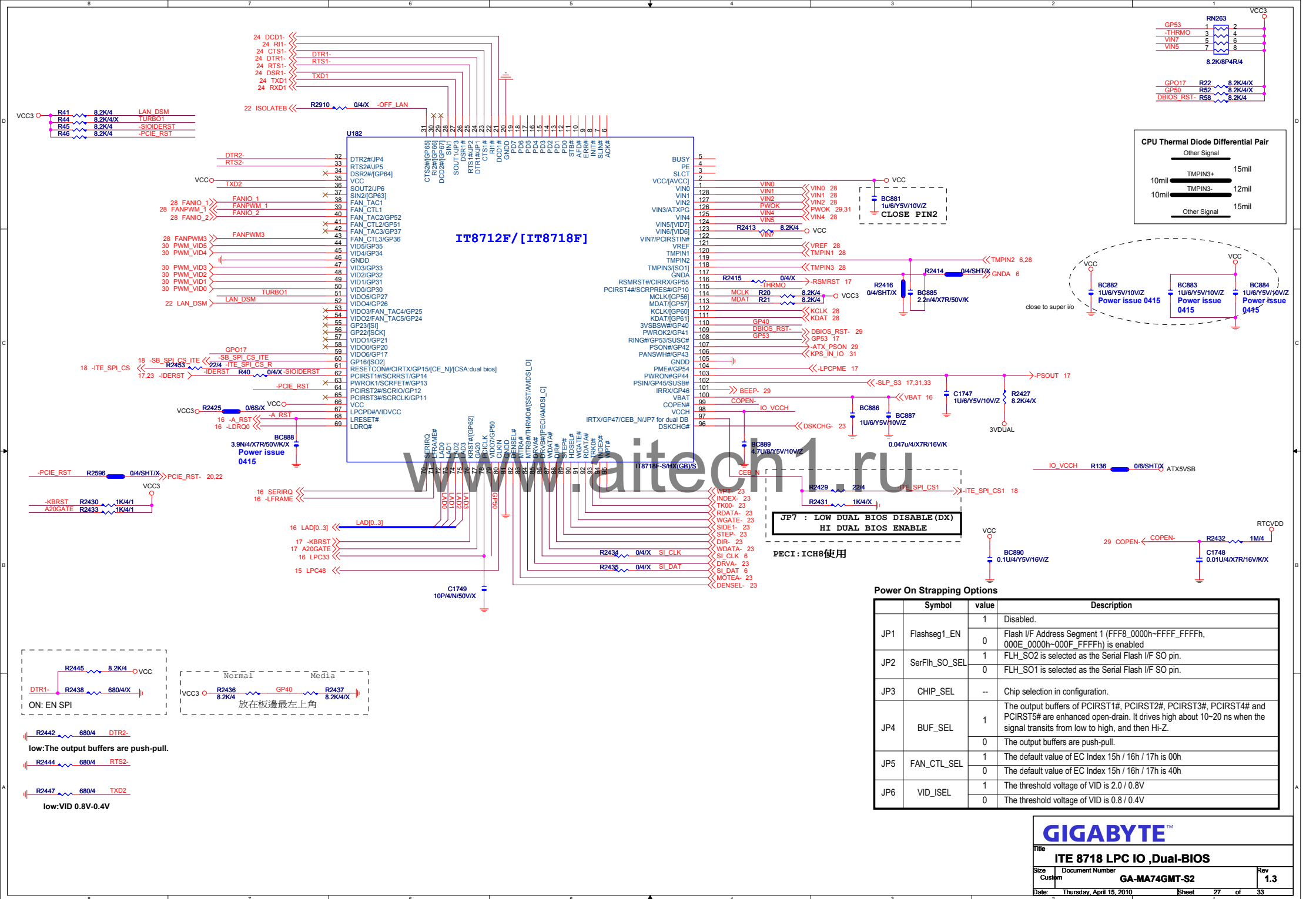
# MIC



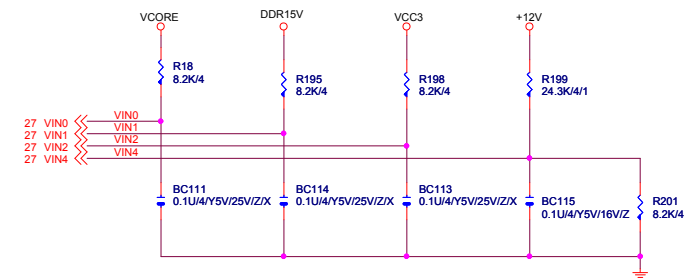
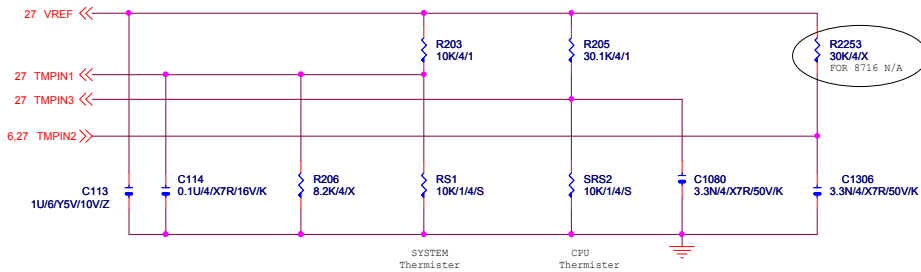
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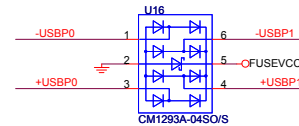
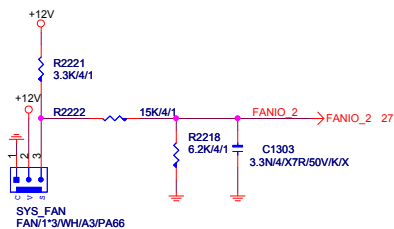
<b>GIGABYTE</b>			
Title <b>AUDIO JACK</b>			
Size	Document Number	Rev	
Custom	<b>GA-MA74GMT-S2</b>	<b>1.3</b>	
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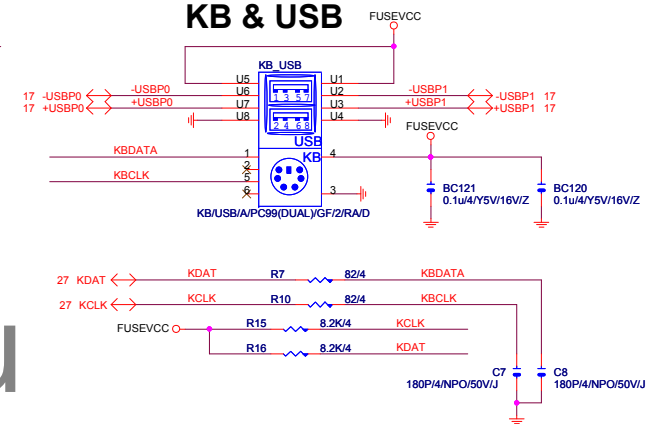
## Hardware Monitor circuits



### SYSTEM FAN

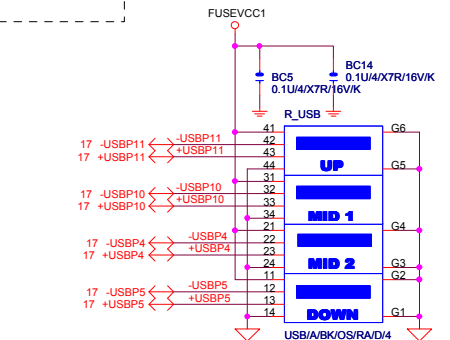
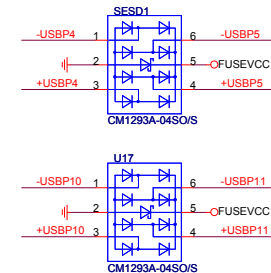
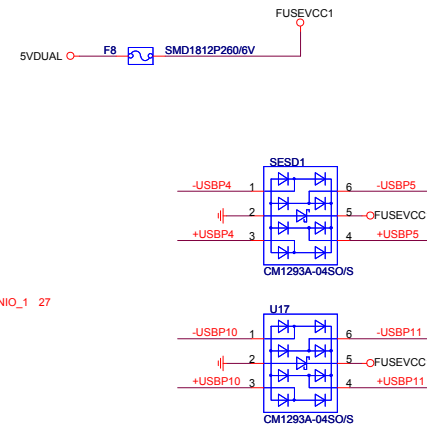
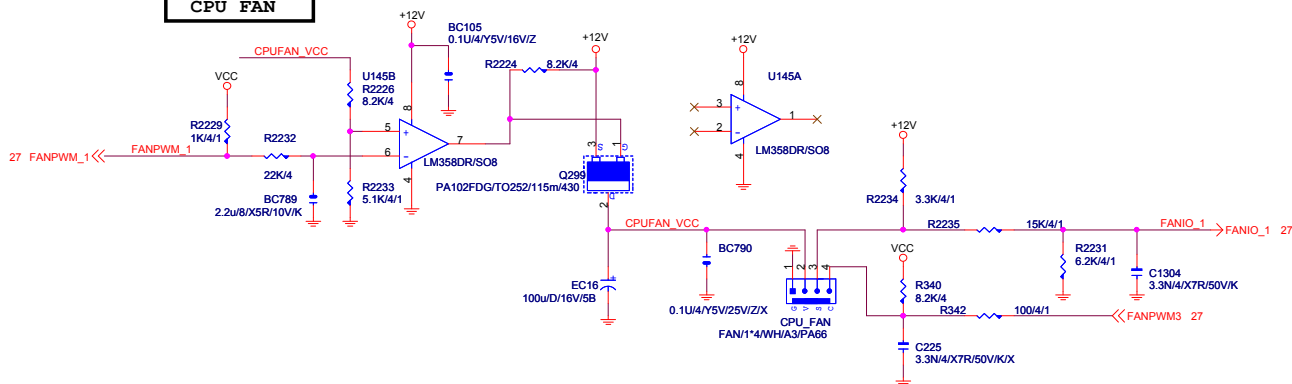


### KB & USB

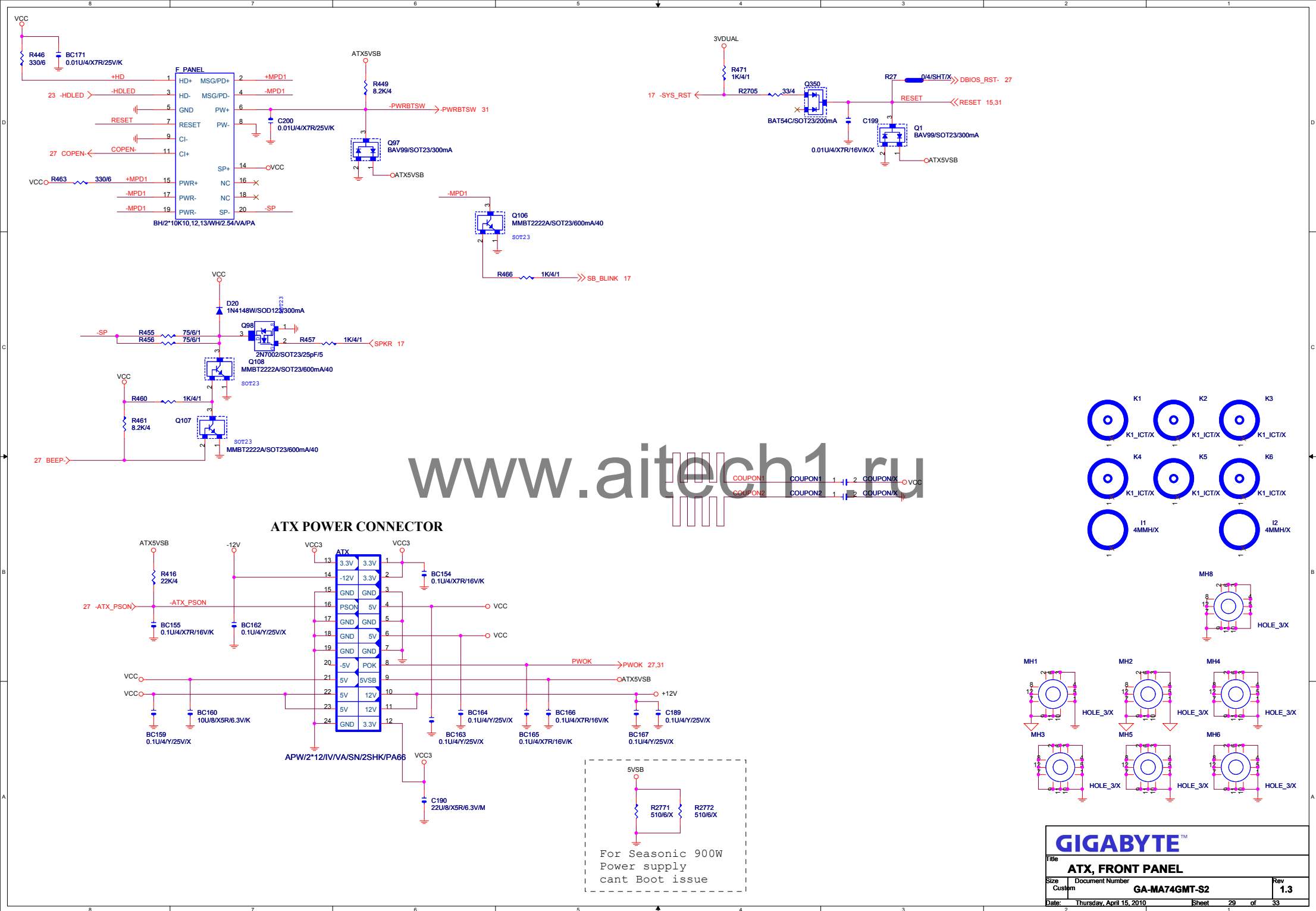


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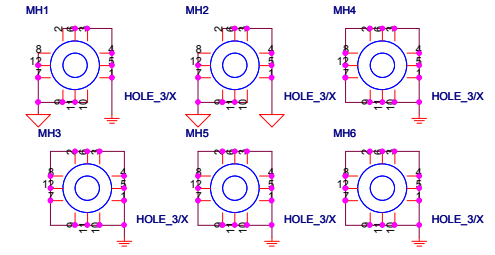
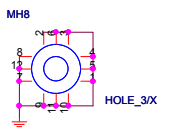
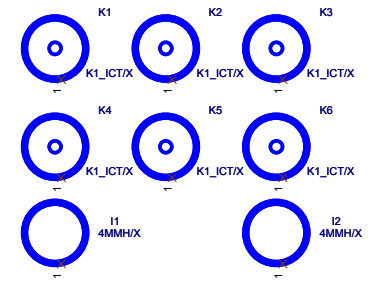
### CPU FAN



GIGABYTE™			
Title <b>FAN/HWMO ,KB/USB</b>			
Size	Document Number	Rev	
Custom	<b>GA-M74GMT-S2</b>	<b>1.3</b>	
Date:	Thursday, April 15, 2010	Sheet	28 of 33

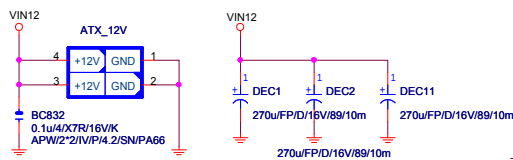


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31 CPUVDD\_EN CPUVDD\_EN R338 0/4/SHT/X 6323\_EN

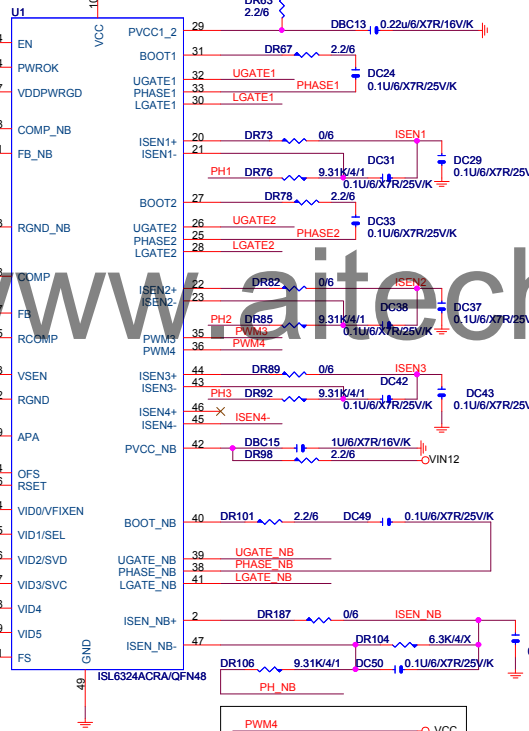
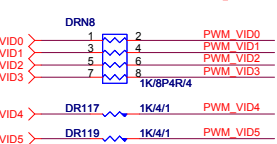
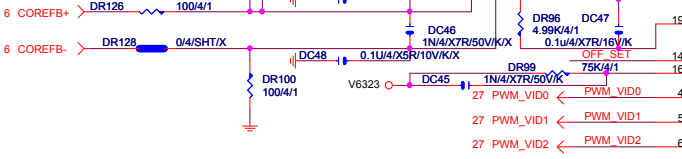
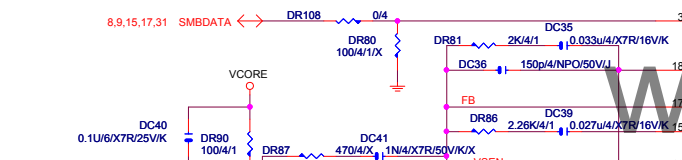
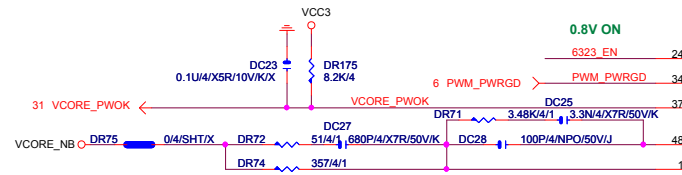
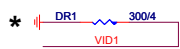
AM2: high, AM2R2: low



**PWROK (SVI)**  
Low : "metal VID"  
High : running protocol

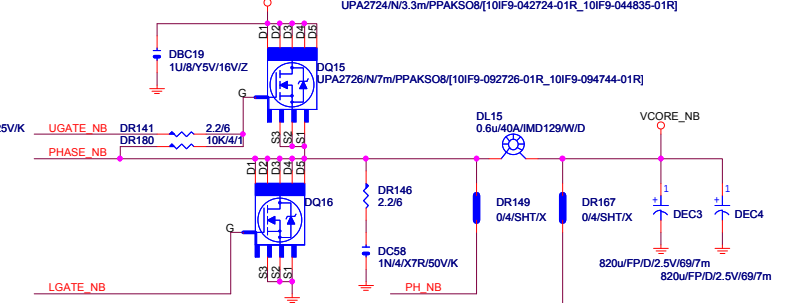
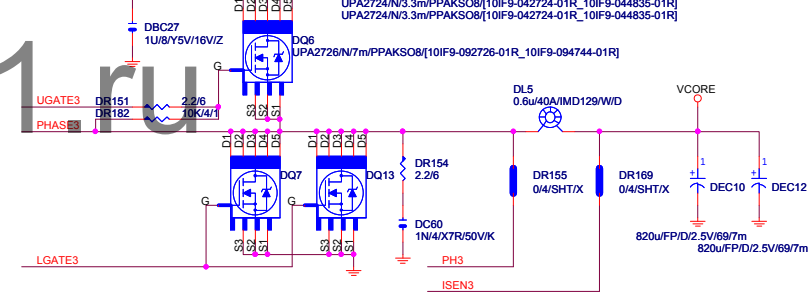
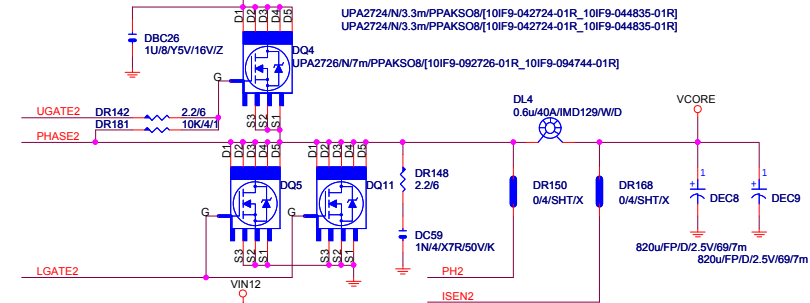
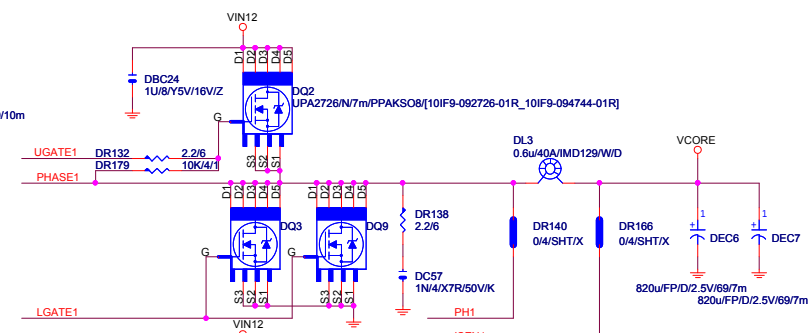
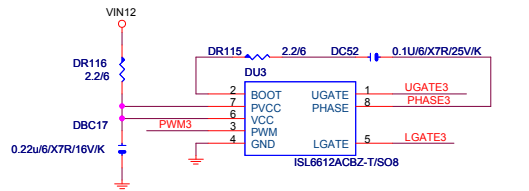
**EN rising edge :**  
Hi : PVI mode  
Low : SVI mode

Pin 34 Input, Pin 37 Output

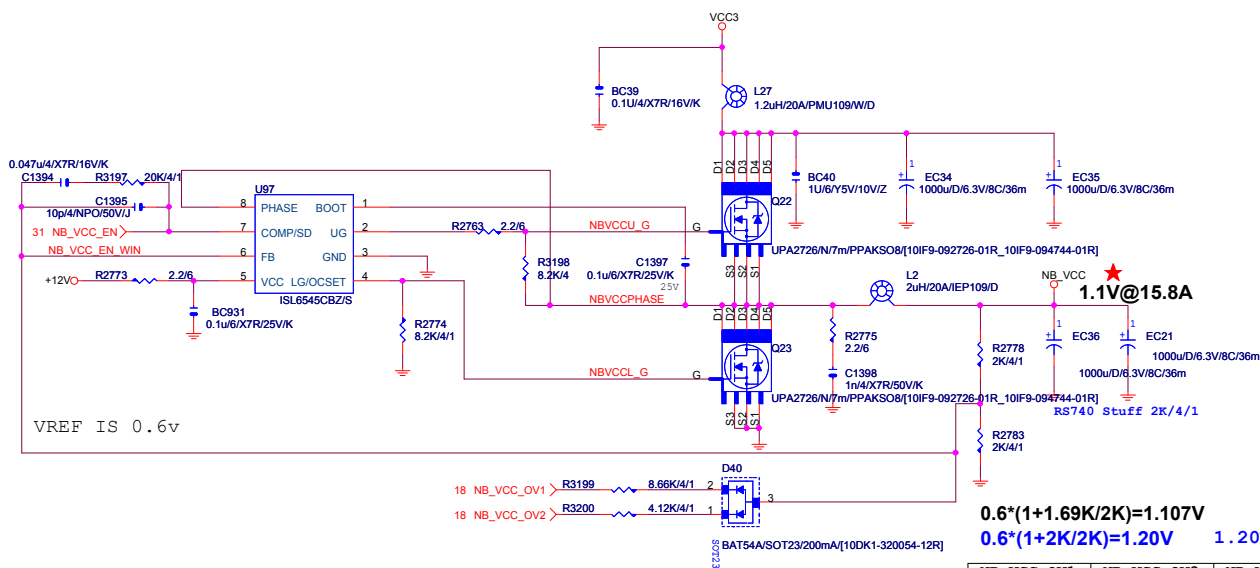


**BOTTOM PAD CONNECT TO GND THROUGH 8 VIA**

**Disable PWM4 Use 3 Phase**



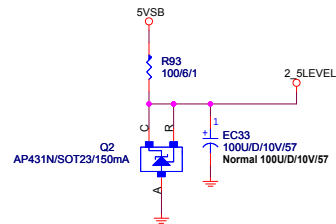




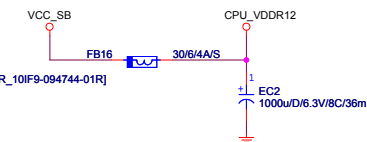
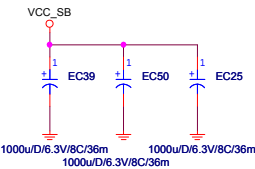
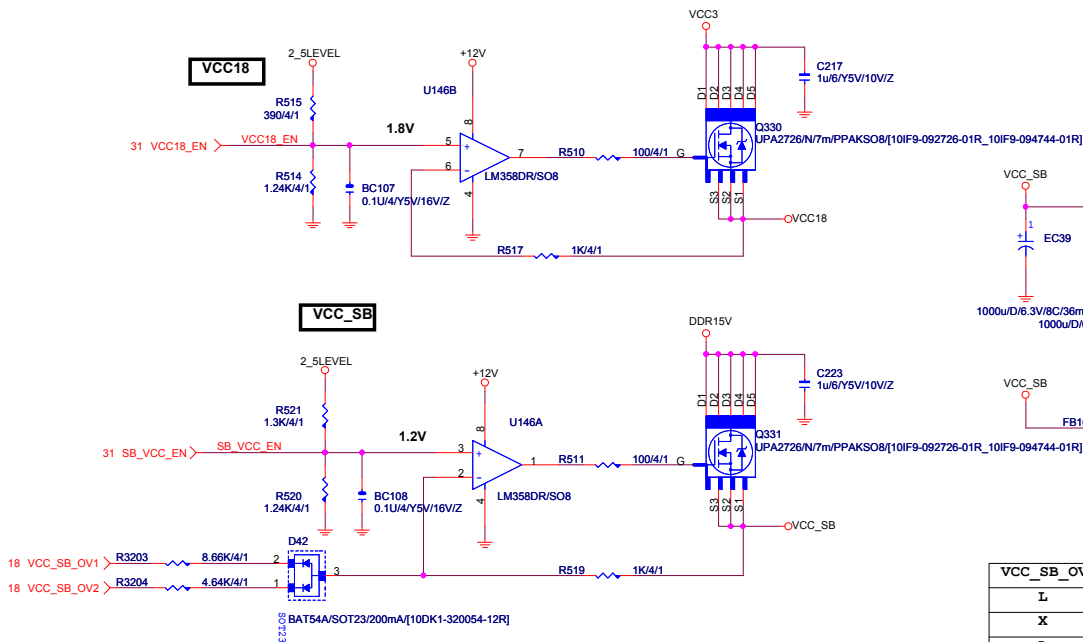
$$0.6 \cdot (1 + 1.69K/2K) = 1.107V$$

$$0.6 \cdot (1 + 2K/2K) = 1.20V \quad 1.20V \text{ for RS740}$$

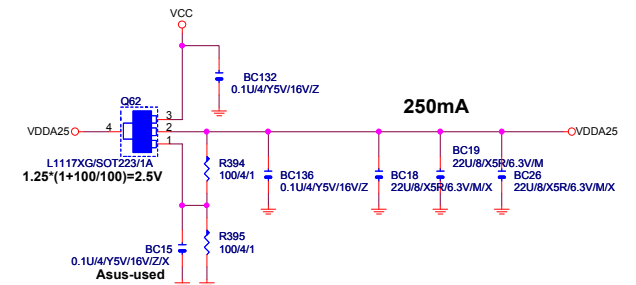
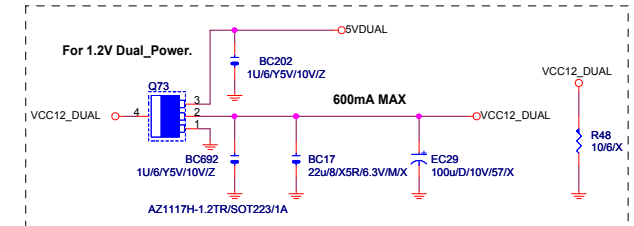
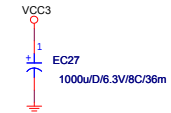
NB_VCC_OV1	NB_VCC_OV2	NB_VCC	NB_VCC
L	X	1.20V	1.30V
X	L	1.30V	1.40V
L	L	1.40V	1.50V



ATI for vcc3/vcc18 power ramp-up 2.1V

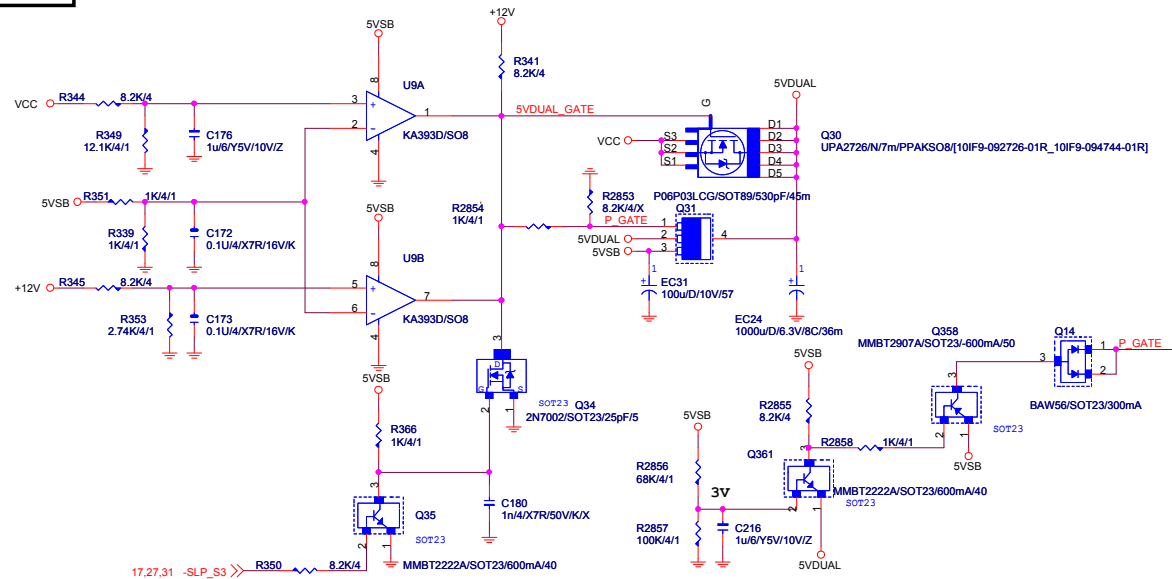


VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

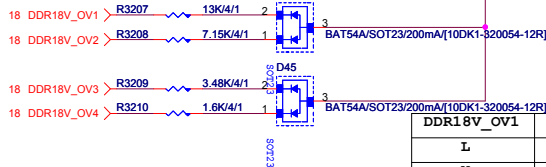
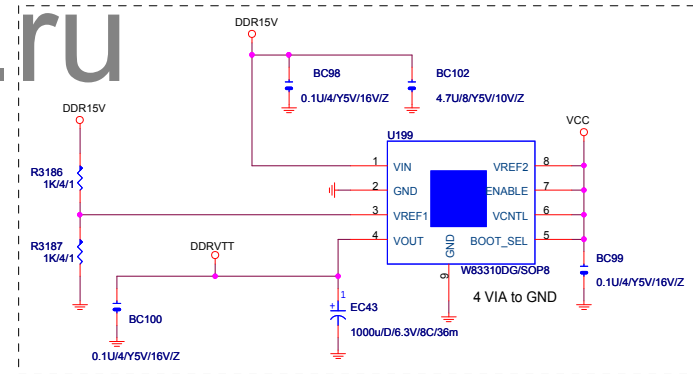
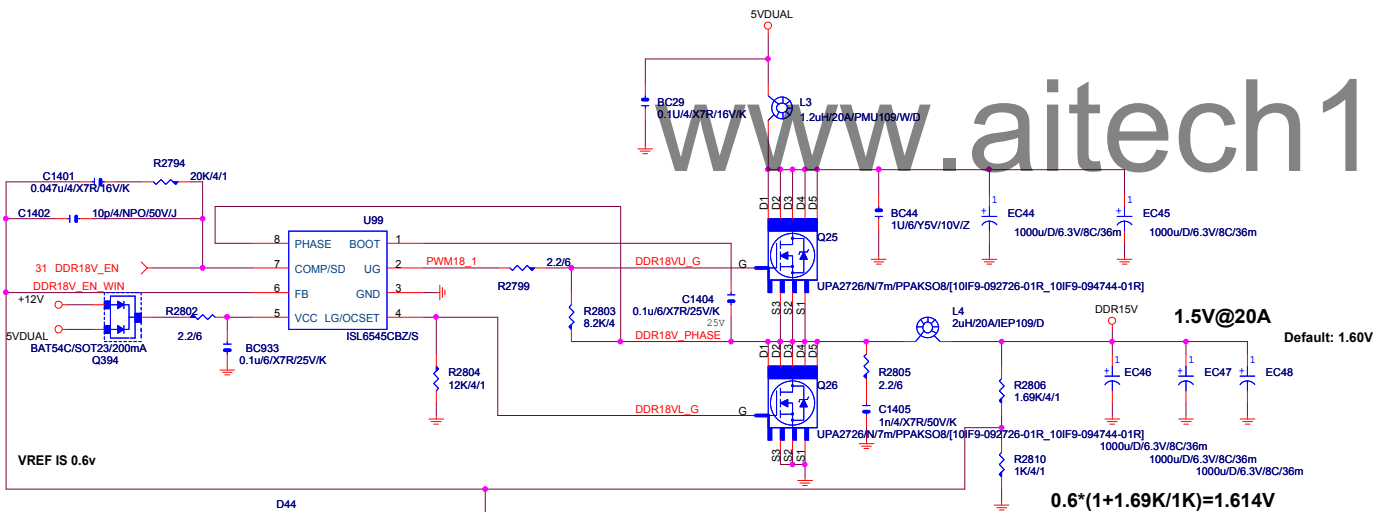
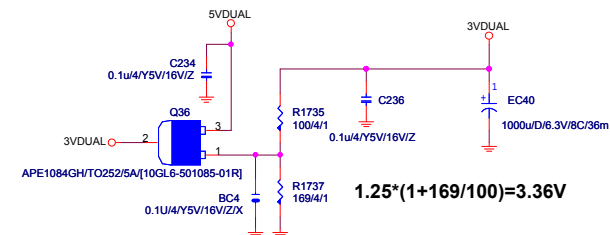




# 5VDUAL



# 3VDUAL



DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
L	X	X	X	1.65V
X	L	X	X	1.70V
L	L	X	X	1.75V
X	X	L	X	1.80V
L	X	L	X	1.85V
X	L	L	X	1.90V
L	L	L	X	1.95V

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
X	X	X	L	2.00V
L	X	X	L	2.05V
X	L	X	L	2.10V
L	L	X	L	2.15V
X	X	L	L	2.20V
L	X	L	L	2.25V
X	L	L	L	2.30V
L	L	L	L	2.35V